

# Scalability and Electrical Properties of Germanium Oxynitride MOS Dielectrics

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**Abstract**—In this letter, we present a fundamental study on the scalability and electrical properties of germanium oxynitride dielectrics for metal-oxide-semiconductor device applications. The nitrogen depth profile within the oxynitride dielectric layers was first monitored using angle-resolved x-ray photoemission spectroscopy and the dielectric permittivity variation was therefore identified. After thinning down the lower permittivity portion of these dielectrics, we successfully scaled down the capacitance-based equivalent SiO<sub>2</sub> thickness, in Ge MOS capacitors, to 1.9 nm without suffering from gate leakage. We have also investigated the effects of thermal annealing on various capacitor electrical properties. For instance, we measured a flat-band voltage shift of as much as  $-0.8$  V from the ideal value on as-deposited capacitors and the recovery of the theoretical value, with acceptably small amount of oxide fixed charge, after subsequent thermal annealing. Lastly, we have benchmarked the performance of these oxynitride insulators with the advanced high- $\kappa$  dielectrics on Ge and discussed the impacts on future scaling.

**Index Terms**—Germanium, metal-oxide-semiconductor (MOS) devices, native dielectric, oxynitride, surface cleaning, surface passivation.

## I. INTRODUCTION

AFTER THE WORK on incorporating high-permittivity (high- $\kappa$ ) dielectric in germanium metal-oxide-semiconductor (MOS) capacitors was published [1], it initiated many research activities on Ge surface passivation and MOS dielectrics [2]–[5]. While most of these studies have claimed to simultaneously solve the instability and nonscalability problems of native Ge dielectrics, a fundamental investigation of these issues has not yet been archived. Such an investigation would additionally improve the understanding of certain high- $\kappa$  dielectric integrations to Ge. For instance, within those high- $\kappa$  dielectric stacks on Ge which are made by chemical vapor deposition (CVD), an intentionally-engineered interlayer composed of oxynitride dielectric would usually be required to guarantee good electrical characteristics [4], [5].

One of the best dielectric candidates on Ge is the oxynitride (GeO<sub>x</sub>N<sub>y</sub>) because it is one of the best known solution to stabilize Ge surfaces, which also enables high-performance Ge MOSFETs with enhanced mobility over Si MOSFETs with

SiO<sub>2</sub> [6]. In addition to its improved thermal and chemical stability over the oxides (GeO and GeO<sub>2</sub>) [7], [8], the incorporation of nitrogen into Ge oxides (like silicon oxynitrides) could effectively suppress any dopant or metal impurities penetrating from the gate electrode through the dielectric, a distinct advantage that would facilitate the integration of novel high- $\kappa$  dielectrics and metal gate electrodes into Ge MOS devices [4], [5]. In this letter, we present a fundamental study on the scalability as well as the electrical properties of the GeO<sub>x</sub>N<sub>y</sub> dielectrics for Ge MOS applications. We also discuss the effects of thermal annealing on these capacitors. Lastly, we benchmark these oxynitride insulators with the advanced high- $\kappa$  dielectrics on Ge.

## II. EXPERIMENTS

MOS capacitors were fabricated on (100) oriented *n*-type Ge substrates with a net background doping concentration of  $\sim 7 \times 10^{15}$  cm<sup>-3</sup>. The substrates were first cleaned by cyclic rinsing between 50:1 HF solution and DI water [5] to remove the native oxides and were then blown dry with nitrogen. Rapid thermal oxidation (RTO) at 500 °C to 600 °C with 5–120 s soak time in dry oxygen was first carried out to form germanium oxides (refractive index of 1.3–1.5) followed by rapid thermal nitridation (RTN) at 600 °C with 1–5 min soak time in ammonia (NH<sub>3</sub>) ambient to convert the oxides into oxynitrides (refractive index 1.5–1.7). NH<sub>3</sub> was chosen as the nitriding agent due to its greater ability to incorporate more nitrogen into the oxynitride film over other species like nitrous oxide (N<sub>2</sub>O) or nitric oxide (NO), as inferred from their behavior on Si oxides. On selected samples, a post-deposition anneal (PDA) at 600 °C for 10 s in dry oxygen was performed. About 50 nm tungsten (W) was subsequently e-beam evaporated through a shadow mask to form gate electrodes of various sizes. Al was then deposited on the wafer backside to reduce the sample contact (and series) resistance. Finally, on the completed W/GeO<sub>x</sub>N<sub>y</sub>/Ge capacitor stacks, thermal anneals were carried out in either dry nitrogen or forming gas (H<sub>2</sub>/N<sub>2</sub>) ambient for 30 min at either 300 °C or 400 °C to investigate their effect on the capacitor electrical properties.

## III. CHARACTERIZATION AND DISCUSSION OF RESULTS

Angle-resolved x-ray photoemission spectroscopy (AR-XPS) was employed to qualitatively depth profile the nitrogen content within the GeO<sub>x</sub>N<sub>y</sub> layer. Illustrated in Fig. 1 is one such profile examining a typical GeO<sub>x</sub>N<sub>y</sub> film. The XPS signals were first peak-fitted around the N(1s) and O(1s) binding energies and the extracted intensities were normalized with their corresponding sensitivity factors. In this film, the nitrogen-to-oxygen XPS

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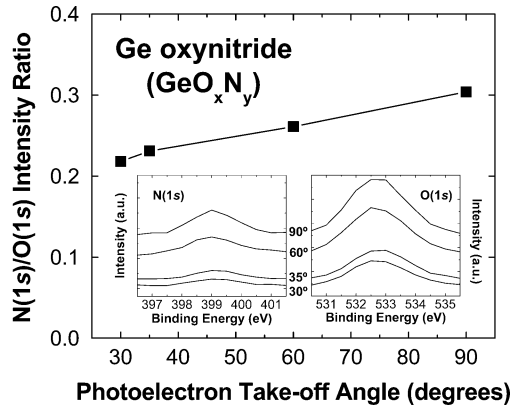


Fig. 1. Angle-resolved X-ray photoemission spectroscopy (AR-XPS) analysis of a typical Ge oxynitride film. The intensity ratio of N(1s) signal to O(1s) signal increases with the photoelectron take-off angle, i.e., higher nitrogen content inside the  $\text{GeO}_x\text{N}_y$  film near the bottom interface. The insets show the N(1s) and O(1s) XPS spectra from different take-off angles.

signal intensity ratio increased with increasing photoelectron take-off angle. In other words, more nitrogen is piled up near the bottom  $\text{GeO}_x\text{N}_y/\text{Ge}$  interface (rather than near the top surface) and raises the local dielectric permittivity. Inspired by this phenomenon, we adopted a general scaling strategy to reduce the initial thermal oxide thickness and thus to trim down the resultant lower- $\kappa$  top surface portion of  $\text{GeO}_x\text{N}_y$ . A secondary approach to scale this dielectric was to increase the degree of nitridation by lengthening the RTN soak time.

Multifrequency capacitance-voltage ( $C-V$ ) characteristics were measured on various  $\text{GeO}_x\text{N}_y$  MOS capacitors. Since, for most of these samples, the amount of frequency dispersion in accumulation was negligible, we extracted the capacitance-based equivalent  $\text{SiO}_2$  thickness (EOT) from the 100-kHz  $C-V$  data. We have demonstrated that this  $\text{GeO}_x\text{N}_y$  could in fact be scaled from an EOT of 11.6–1.9 nm without suffering from gate leakage induced  $C-V$  distortion [9]. Fig. 2(a) illustrates the  $C-V$  characteristics from a typical W-gate Ge MOS capacitor with a  $\text{GeO}_x\text{N}_y$  dielectric measured before and after thermal anneals. After a thermal anneal at 300 °C (in  $\text{N}_2$  and then in forming gas), both the EOT and  $C-V$  hysteresis increased slightly from 3.25 to 3.45 nm and 25 to 35 mV, respectively. In addition, a distinct positive flatband voltage ( $V_{\text{FB}}$ ) shift of about 0.8 V can be seen. The kinks that showed up near inversion in lower frequency scans suggest the presence of slow interface states, even after various thermal anneals. Also shown in Fig. 2(b) is the corresponding gate leakage density as a function of voltage bias for both gate and substrate injections. The seemingly lower leakage current was observed after thermal anneals which will be discussed in the following sections.

To further investigate the effects of thermal annealing on capacitor  $V_{\text{FB}}$  shift, after each annealing treatment we monitored the  $V_{\text{FB}}$  on many capacitors which are summarized in Fig. 3. For reference purposes, the ideal  $V_{\text{FB}}$  (assuming zero oxide fixed charge density,  $Q_f$ ) and the theoretical  $V_{\text{FB}}$  (assume an arbitrary EOT of 4.0 nm and  $Q_f$  of  $10^{12}$  C/cm<sup>2</sup>) are also included. On the as-deposited capacitors, a positive  $V_{\text{FB}}$  shift of 0.6–0.8 V could be measured after an initial 300 °C anneal in  $\text{N}_2$ . On these treated samples, a subsequent forming gas anneal

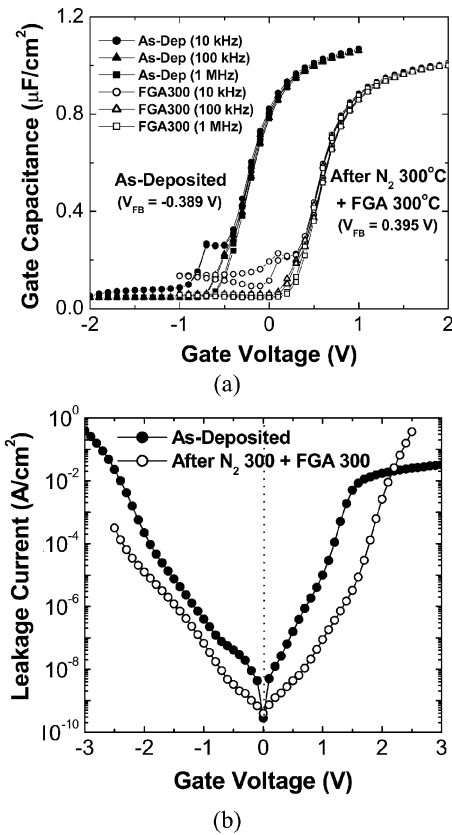


Fig. 2. (a) Multifrequency gate capacitance-voltage characteristics measured from an as-deposited W/ $\text{GeO}_x\text{N}_y/\text{Ge}$  capacitor stack (solid symbols) and after 300 °C anneal in  $\text{N}_2$  and then in forming gas (open symbols). The interface trap density reduced from  $8 \times 10^{12}$  cm<sup>-2</sup>eV<sup>-1</sup> to  $3 \times 10^{12}$  cm<sup>-2</sup>eV<sup>-1</sup> after the anneals. (b) The corresponding gate leakage-voltage measurements.

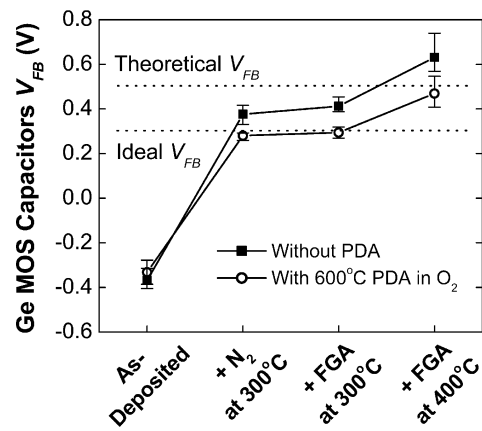


Fig. 3. Changes of W/ $\text{GeO}_x\text{N}_y/\text{Ge}$  capacitor (with 3.0–5.0 nm EOT) flat-band voltage after subsequent anneals in either  $\text{N}_2$  or forming gas ambient at either 300 °C or 400 °C for 30 min. Solid and open symbols, respectively, represent  $\text{GeO}_x\text{N}_y$  samples without and with oxygen PDA prior to W deposition. The ideal  $V_{\text{FB}}$  (assuming zero oxide fixed charge density) and the theoretical  $V_{\text{FB}}$  (assuming an EOT of 4.0 nm and oxide fixed charge density of  $10^{12}$  C/cm<sup>2</sup>) are also included.

at 300 °C only increased the  $V_{\text{FB}}$  minimally; however, a succeeding anneal at 400 °C in forming gas conversely raised the  $V_{\text{FB}}$  by an extra 0.2–0.3 V. We noticed that the theoretical  $V_{\text{FB}}$  with small amount of oxide fixed charge (e.g.,  $10^{12}$  C/cm<sup>2</sup>) was achieved experimentally only after thermal anneals at 300 °C

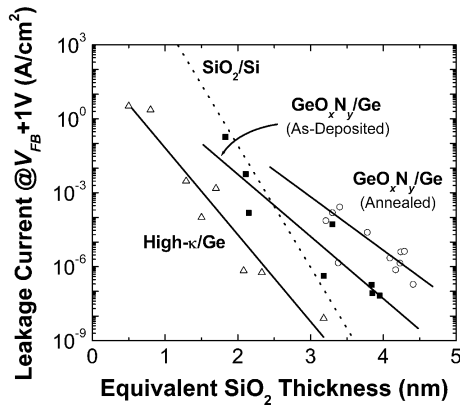


Fig. 4. Benchmarking the gate leakage density (normalized at 1 V above flat-band voltage) as a function of EOT for the  $\text{GeO}_x\text{N}_y$  and high- $\kappa$  dielectrics on Ge MOS capacitors. All the data were measured on  $n$ -type Ge substrate. As a reference the leakage current level from thin  $\text{SiO}_2$  on the Si MOSFET is also included.

and above. This could be attributed to the elimination of radiation charging occurring during W e-beam evaporation. On the annealed capacitors, we observe the characteristic positive  $V_{\text{FB}}$  shift from the ideal value due to positive  $Q_f$  generation during RTN. Meanwhile, the oxygen PDA at 600 °C was shown to reduce the amount of  $Q_f$  inside the  $\text{GeO}_x\text{N}_y$  layer, but that would also increase the dielectric EOT.

In order to evaluate the performance of these  $\text{GeO}_x\text{N}_y$  dielectrics more representatively, we have benchmarked their gate leakage density (normalized at 1 V above  $V_{\text{FB}}$ ) as a function of EOT (Fig. 4) with the published data on Ge MOS capacitors with high- $\kappa$  dielectrics [1],[3]–[5]. As a reference, the gate leakage current for thin  $\text{SiO}_2$  on the Si MOSFET [10] is also included. From both the as-deposited and annealed  $\text{GeO}_x\text{N}_y$  dielectrics on Ge, an expected exponential increase of gate leakage with decreasing EOT could be observed. In contrast to the higher gate leakage [Fig. 2(b)] owing to the negatively shifted  $V_{\text{FB}}$  of the as-deposited samples (discussed in Fig. 3), the normalized gate leakage shown in Fig. 4 of the annealed samples is in fact higher than that of the as-deposited case. When these annealed  $\text{GeO}_x\text{N}_y$  are compared to the high- $\kappa$  on Ge, about four to five orders of magnitude higher gate leakage could be revealed. To the best of our knowledge, this is the first exhibition of effective gate leakage suppression at a given EOT value upon replacing the  $\text{GeO}_x\text{N}_y$  dielectrics with high- $\kappa$  on Ge. Lastly, it should be noted that by extrapolating both the annealed  $\text{GeO}_x\text{N}_y$  and high- $\kappa$  curves backward, they would intersect at a very low EOT value as the interlayer thickness. This may imply that the  $\text{GeO}_x\text{N}_y$ , which acted as a sub-nanometer interlayer in high- $\kappa$  gate stack on Ge [4], [5],

should allow the scaling of certain high- $\kappa$  dielectric stacks on Ge more than high- $\kappa$  on Si with usually thicker interlayer. To continue the effective device scaling, further investigations of the Ge interface and surface preparations are undoubtedly indispensable.

#### IV. CONCLUSION

In conclusion, we have performed a fundamental study on the scalability as well as the electrical properties of the Ge oxynitride dielectrics for MOS applications. We have also investigated the effects of thermal annealing on these capacitors. Lastly, we have benchmarked these oxynitride insulators with the advanced high- $\kappa$  dielectrics on Ge.

#### ACKNOWLEDGMENT

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